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Novel Energy Efficient One Bit Full Adder / Subtractor

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Abstract: In this work one bit Full Adder/Subtractor with Twentyfour and Fourteen transistors have been proposed. Reducing Power dissipation, supply voltage, leakage currents, area of chip are the most important parameters in today`s VLSI designs. The system reliability can be increased by reducing the cost, weight and physical size and it is achieved by decreasing the transistor count. Therefore the minimum power consumption target and lower area can be meet by reducing the hardware size. Digital circuits can be minimize in two methods. One is human method and another is Computational method. This paper propose one-bit Full Subtractor based on human method with twenty and fourteen transistors and simulation for the designed circuits were also performed with "MENTOR GRAPHICS TOOL" .

Index Terms- 24T full adder-subtractor, 14T full adder-subtractor, Delay, Power Dissipation, Area.

I INTRODUCTION

In recent trends, low-power design has become a major design constraint. To design a full adder-subtractor the transistor count is an important concern which widely affects the design complexity of ALU and other functional units.

Also propagation delay plays a very important role in the design and synthesis of VLSI circuits. Speed of the design is limited by number and size of the transistors, parasitic capacitance and delay in the critical path. The driving capability of a full adder -subtractor is very important, as they are mostly used in cascade configuration, where the output of one drives the input for other.

Reducing the supply voltage appears to be the most eminent means to reduce the power consumption [1]. Reducing supply voltage also increases the circuit delay. So our goal is to achieve low-power and high speed circuit design. As area of the circuit is also an important parameter in low-power design, here we have studied the parametrical analysis with 14T full adder-subtractor circuit which has very low area, having very less number of transistors.

II DESIGN OF FULL CONVENTIONAL ADDER / SUBTRACTOR

A basic Complementary Metal Oxide Semiconductor gate is a mixture of two networks, one is pull up and another is pull down network. The pull up network which is constructed using PMOS devices and the pull-down network is constructed using NMOS devices as shown in Fig.1. The primary reason for this choice is that NMOS transistors produce "strong zeroes" and PMOS devices generate "strong ones". The function of the pull up network is to establish a connection between the output and supply voltage (VDD) anytime the output of the logic gate is meant to be 1 (based on the inputs).

Similarly the function of the pull down network is to connect the output to ground (VSS) when the output is meant to be 0. Static logic retain its output level as long as the power is applied. Generally outputs are generated in response to input voltage levels after a certain time delay. In static logic design, any combinational design will possess an equal number of PMOS and NMOS transistors.

Conventional Full Adder / Subtractor is a combinational logic circuit which performs addition & subtraction between two bits.

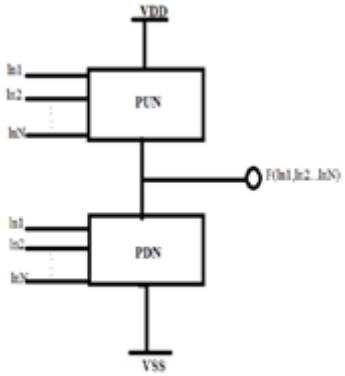


Fig.1. StaticCMOS Circuit.

III PROPOSE 24T FULL ADDER / SUBTRACTOR

Fig. 2 shows the transistor level circuit diagram of Full Adder/Subtractor with twenty four transistors with MENTOR GRAPHIC TOOL. It consumes less power and low leakage current and occupies less area due to the number of transistors count reduced when compared to static CMOS Full Adder/Subtractor. Here six transistors used for implementing difference equation and ten transistors for borrow equation while rest of four transistors for inverting operation.

IV PROPOSED 14T FULL ADDER / SUBTRACTOR

The 14T full adder-subtractor is designed by using the 10T full adder logic. Here both the addition and the subtraction is done simultaneously. But the control unit controls the logical functioning of the circuit.

As for a full adder or full subtractor the generalized expression for the sum and the difference is same. Two XOR gates are designed using pass transistor logic to obtain the SUM or DIFFERENCE output. The expression for SUM/DIFF is given below in eqn (1)

SUM/DIFF = A xor B xor C …..(1)

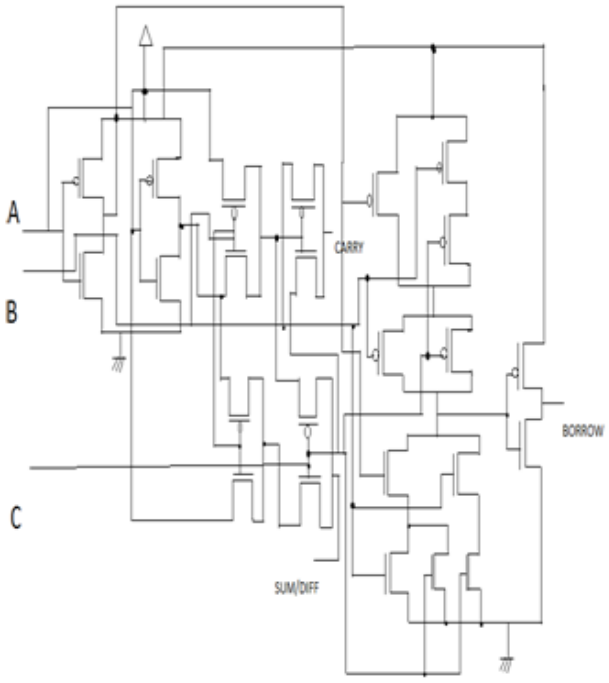


Fig 2:- Proposed 24T Full Adder / Subtractor

The CARRY and BORROW signals are generated by using pass transistor logic. The expression used for CARRY and BORROW are given below in eqn (2) and eqn (3)

CARRY = A.B + (Axor B) .C …..(2)

BORROW = (A xor B) .C + A.B …..(3)

The CARRY and the BORROW signals are then fed to a separate controlling pass transistor pair, where a controlling gate voltage controls the circuit operation. This control voltage determines when the addition orthe subtraction operation will take place. If, the control voltage is logic ‘0’ then the generated CARRY signal will be generated as the final output result and hence addition operation will be performed. Similarly, if the control voltage is logic ‘1’ then the BORROW signal will be generated as the final output to complete the subtraction operation. The schematic diagram of the proposed 14T full adder/ subtractor is shown in Fig.3

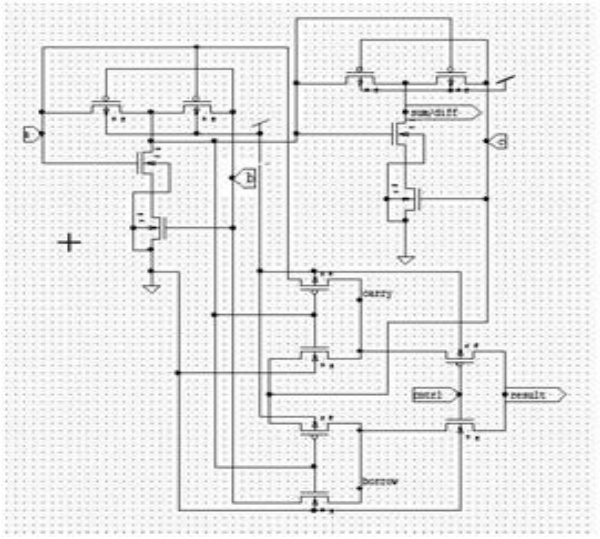


Fig.3: Proposed 14T Full Adder / Subtractor

V SIMULATION RESULTS

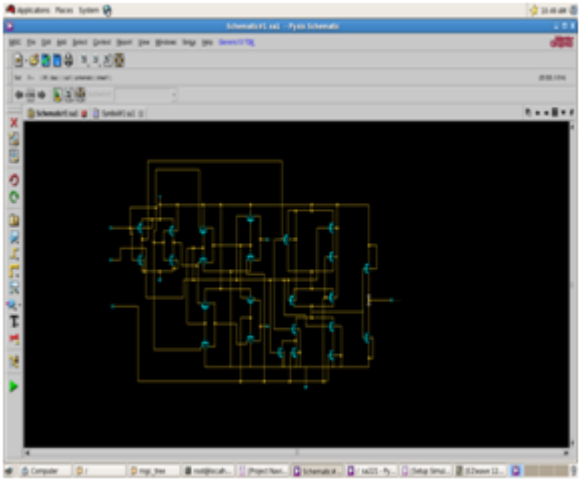


Fig 4 :- Schematic Diagram of 24T full adder/ subtractor

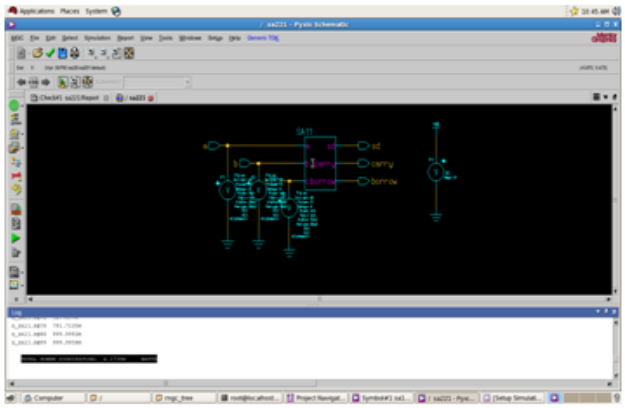


Fig 5:- Symbol of 24T full adder/subtractor

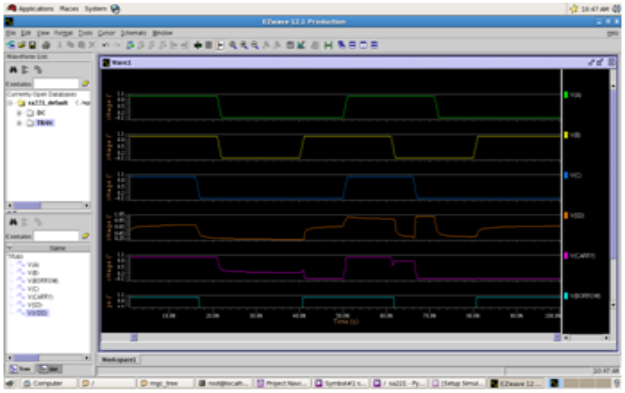


Fig 6:- Wave form of 24T full adder/subtractor

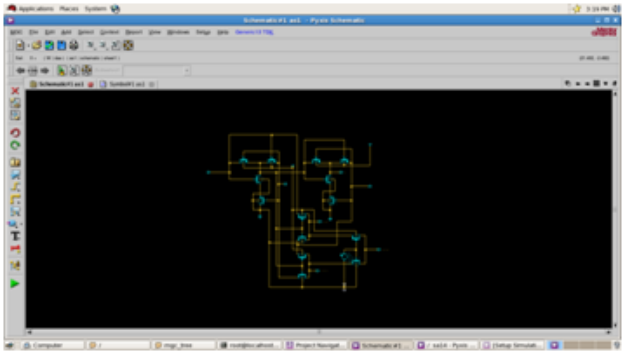


Fig 7:- Schematic diagram of 14T full adder/subtractor

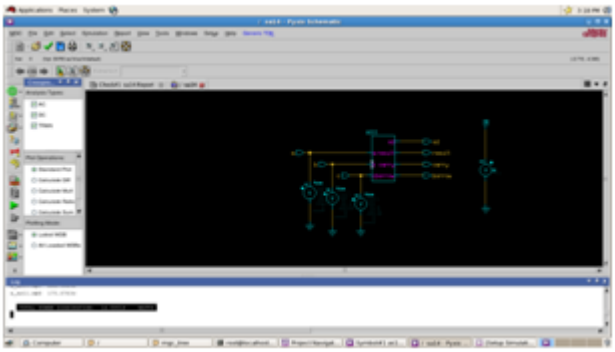
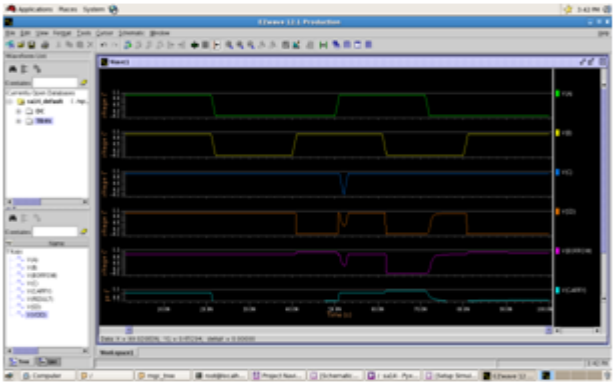


Fig 8:- Symbol of 14T full adder/subtractor



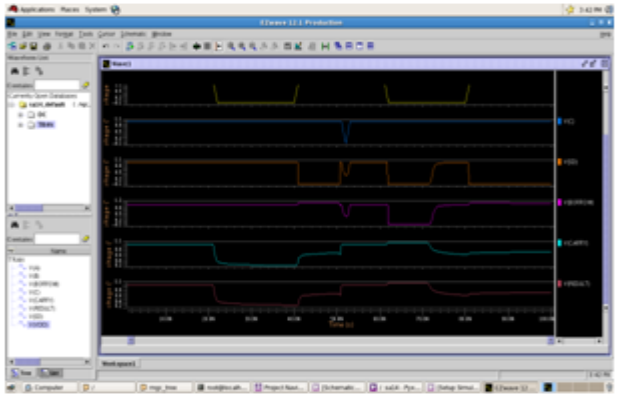


Fig 9:- Waveforms of 14T full adder/subtractor

VI CONCLUSION

Table: Power analysis of various types of Full Adder/ Subtractor

CIRCUIT	POWER
28T FULL ADDER	2.2286 nw
40T FULL SUBTRACTOR	6.5336 nw
24T FULL ADDER/SUBTRACTOR	4.1739 nw
14T PROPOSED FULL ADDER/SUBTRACTOR	14.0001 pw

From above table we can see the variation in the power dissipation .When we designed 28T full adder we get the power of 2.2286nw,for 40T full subtractor we get as 6.533nw.But by combining this to we get 8.76nw so more power consumption is occurred & also more area is occupied. To lessen these parameters we designed 24T full adder/subtractor we get 4.1739nw.Still there is chance to reduce power consumption & area so we designed 14T full adder/subtractor we get power as 14.0001pw

So by reducing transistor count we can reduce the power consumption & area occupation.

VII ACKNOWLEDGEMENT

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