

Neural Modified Karnaugh Map for Boolean Circuit

P. Murugavel,
Assistant Professor, Department of Computer Science,
Joseph Arts and Science College, Thirunavallur, Villupuram.

Abstract: A shortcut hand reduction method known as Karnaugh Map. It is an efficient way of reducing boolean function to a minimum form For the purpose of minimizing hardware requirements. Karnaugh Map is an efficient method of minimization for conventional logic design. It is used for 3 or 4 variables at most 6 variable. In our proposed system we modify the karnaugh map and propose a set of reduction rules for quantum boolean circuit optimization. By applying these rules we can efficiently simplify a quantum boolean circuit that has an arbitrary number of input variables. For this we propose an algorithm to simplify logic functions with any number of variables by using the modified karnaugh Map.

Keywords- Boolean Algebra, Karnaugh Map

I. INTRODUCTION

A Neural Network is a system of programs and data structures that approximates the operation of the human brain. A neural Network usually involves a large number of processors operating in parallel. A Neural network is initially trained about data relationship. Neural network use several principles, including gradient based training, fuzzy logic, genetic algorithm, Bayesian Methods.

Karnaugh Map is an efficient method of minimization for conventional logic design. It is used for 3 or 4 variables at most 6 variable. In our proposed system we modify the karnaugh map and propose a set of reduction rules for quantum boolean circuit optimization[5]. By applying these rules we can efficiently simplify a quantum boolean circuit that has an arbitrary number of input variables. For this we propose an algorithm to simplify logic functions with any number of variables by using the modified karnaugh Map.

The author Arunachalam Solairaju simplify the logic function, we can reduce the original number of digital components (gates) required to implement digital circuits, therefore by reducing the number of gates, the Chip size and cost will be reduced and the computing speed will be increased [7].

A new fast simplification method is presented. Such method realizes karnaugh map with large number of variables. In order to accelerate the operation of the proposed method, a new approach for fast detection of group of ones is presented. Such approach implemented in the frequency domain. The search operation relies on performing cross correlation in the the frequency domain rather than time one. It is proved mathematically and practically that the number of computation steps required for the presented method is less than that needed by conventional cross correlation[1]. Simulation results using MATLAB confirm the theoretical computations.

II. WHY ARTIFICIAL NEURAL NETWORK

- Massive parallelism
- Distributed representation and computation

- Learning ability
- Generation ability
- Adaptivity
- Inherent contextual information processing
- Fault tolerance and
- Low energy consumption

III. OBJECTIVES OF THE THESIS

- Minimum number of Literals
- Elimination of gates
- Reduction time is minimum
- Cost becomes reduced
- This method is very simple
- Tabulation method can also be simplified with minimum time.

IV. MODIFIED KARNAUGH MAP AND THE CIRCUIT OF A FULL ADDER

- Karnaugh map is used as a method for minimizing a Boolean expression. It is usually aided by a rectangular map of the values of the expression for all possible input combinations.
- Input values are arranged in a Gray code, which is an ordering of 2 power n binary number such that only on bit changes from one entry to the next.
- The methods for construction of full adder using k-map is as shown in the fig 1.

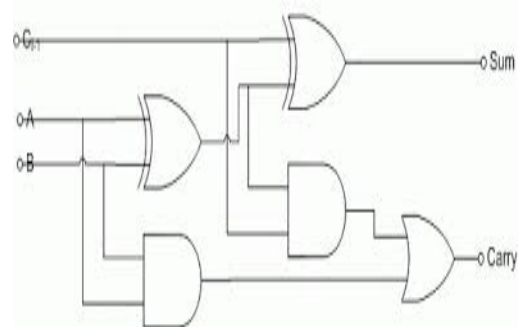


Figure1: Full Adder Using K-Map

- Full adder is a combinational circuits that can add three bits. The circuits consists of two half adders and one OR gate.
- The output of OR gate is the carry and the output of second XOR gate is the sum.
- The k-map for sum and carry is as shown in the fig 2, it is possible that more than one reduction rules can be applied at the same time, so we need a mechanism to estimate the cost of each selection [8,9].

References

[1] A. Barenco, C.H. Bennett, R.Cleve, D.P. Divincenzo, N.Margolas, short.Sleator, J.A.Smolin and H. Weinfurter, "Elementary gates quantum Computations," pp.3457 -3467, 1995.
 [2] Steven M.Nowick and David L Dill, Member, IEEE "Exact two-Level Minimization of Hazard-Free Logic with Multiple-input Changes".Designs of Integrated Circuit And System Vol 14.No.8, Aug 1995
 [3] O.Ledion Bitincke, George E. Antoniou, "PDA – Based Boolean Function Simplification: A useful Education Tool" Informatika, 2004, Vol.15, no.3, pp.329 -336.
 [4] Ledion Bitincke, George E. Antoniou, "Pocket – Pc Boolean Function Simplification", Journal of Electrical Engineering, Vol.56, No. 7-8, 2005, pp 209-212.
 [5] I – Ming Tsai and sy– yen. Kuo, "Quantum Boolean Circuit construction and layout under locality constraint", in proc. Of the 1st IEE Conference on Nanotechnology, 2001, pp 111 -116.
 [6] Hazem M.Bakry, Ahmed Atwan, Department of information system "Simplification and implementation of boolean function" Jan 2010, International Journal of Computer Science Vol1 2010, pp 41-0
 [7] Arunachalam Solairaju ,Rajupillai Periyasamy "Optimal Boolean Function Simplification through K- MapUsing object-Oriented Algorithm" Journal of International,Computer Application Vol 15.No.7, Feb 2011
 [8] Dr.Vipin Saxena, Manish Shrivastava and Dr.Deepak Arora "Performance Estimation of Karnaugh Map through UML" International Journal of Computer Science and Network Security, Vol 9, No.6, June 2009
 [9] Fatih Basciftci, and Halan Akar "Finding isolated minterms in simplification of logic functions" International Conference on challenges in IT,Engineering and Technology (ICCIET 2014)July 17-18,2014 Phuket (Thailand)

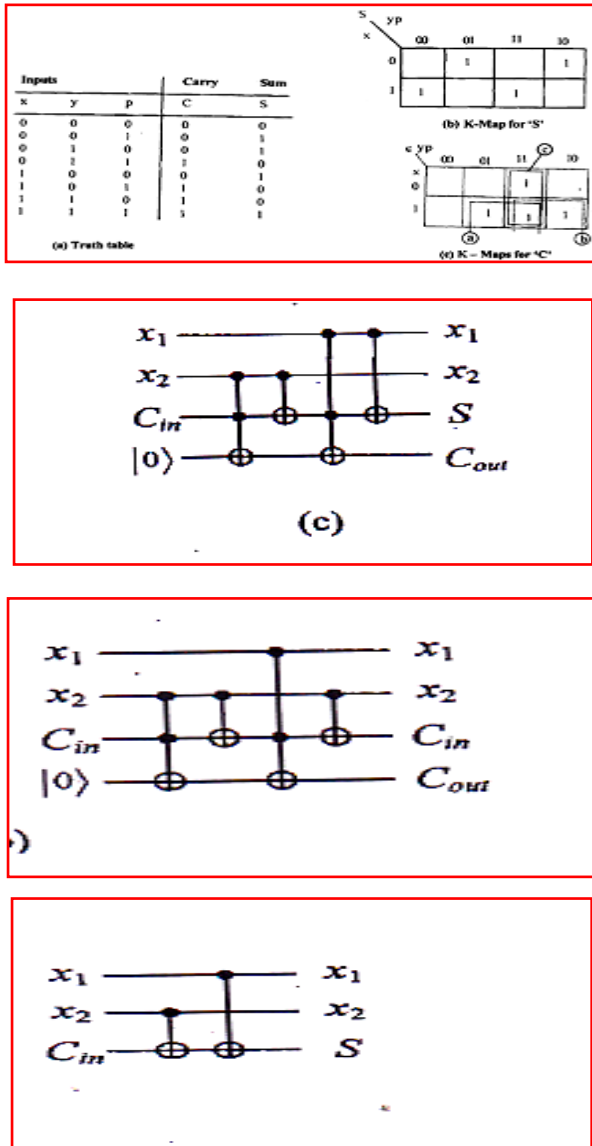


Figure 2: The K-Map for Sum And Carry

V. RESULT AND DISSCUSSION

We modify the karnaugh map and propose a set of reduction rules for quantum Boolean circuit optimization [2,3,4,6]. Always combine as many cells in a group as possible. This will result in the fewest number of literals in the term that represents the group. Make as few groupings as possible to cover all minterms. This will result in the fewest product terms. Always begin with the largest group, which means if you can find eight members group is better than two four groups and one four group is better than pair of two-group.

By applying these rules, we can efficiently simplify a quantum Boolean circuit. A shortcut hand reduction method known as Karnaugh Map.

CONCLUSION

In this paper, we have proposed an algorithm that transforms an original truth table into a quantum Boolean circuit. With our algorithm, we can reduce not only the number of quantum gates but also the basic operations of the circuit.